PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = VARTTI
First Name = KELVIN

Application#	Patent#	Status	Date Filed	Title	Inventor Name 22
10926250	Not Issued	030	08/25/2004	METHOD AND APPARATUS FOR PROVIDING OVERLAPPING DEFER PHASE RESPONSES	VARTTI, KELVIN S.
10620515	Not Issued	030	07/16/2003	PROGRAMMABLE SYSTEM AND METHOD FOR ACCESSING A SHARED MEMORY	VARTTI, KELVIN S.
10620406	Not Issued	030	07/16/2003	PROGRAMMABLE CACHE MANAGEMENT SYSTEM AND METHOD	VARTTI, KELVIN S.
10601030	Not Issued	030	06/20/2003	SYSTEM AND METHOD FOR HANDLING MEMORY REQUESTS IN A MULTIPROCESSOR SHARED MEMORY SYSTEM	VARTTI, KELVIN S.
10600880	Not Issued	030	06/20/2003	SYSTEM AND METHOD FOR MAINTAINING MEMORY COHERENCY WITHIN A MULTI-PROCESSOR DATA PROCESSING SYSTEM	VARTTI, KELVIN S.
10600205	Not Issued	030	06/20/2003	DATA ACCELERATION MECHANISM FOR A MULTIPROCESSOR SHARED MEMORY SYSTEM	VARTTI, KELVIN S.
10255495	Not Issued	041	09/26/2002	SYSTEM AND METHOD FOR INITIALIZING MEMORY WITHIN A DATA PROCESSING SYSTEM	VARTTI, KELVIN S.
10255393	Not Issued	041	09/26/2002	DATA PRE-FETCH SYSTEM AND METHOD FOR A CACHE MEMORY	VARTTI, KELVIN S.
10255276	Not Issued	094	09/26/2002	DELAYED LEAKY WRITE SYSTEM AND METHOD FOR A CACHE MEMORY	VARTTI, KELVIN S.
10160947	6816952	150	05/31/2002	LOCK MANAGEMENT SYSTEM	VARTTI, KELVIN S.

				AND METHOD FOR USE IN A DATA PROCESSING SYSTEM	
09750637	6625698	150	12/28/2000	METHOD AND APPARATUS FOR CONTROLLING MEMORY STORAGE LOCKS BASED ON CACHE LINE OWNERSHIP	VARTTI, KELVIN S.
09748535	6697925	150	12/22/2000	USE OF A CACHE OWNERSHIP MECHANISM TO SYNCHRONIZE MULTIPLE DAYCLOCKS	VARTTI, KELVIN S.
09707625	Not Issued	041	11/07/2000	SYSTEM AND METHOD FOR INCREASING CACHE HIT DETECTION PERFORMANCE	VARTTI, KELVIN S.
09651598	6799249	150	08/30/2000	SPLIT CONTROL FOR IP READ AND WRITE CACHE MISSES	VARTTI, KELVIN S
09651597	Not Issued	095	08/30/2000	METHOD FOR AVOIDING DELAYS DURING SNOOP REQUESTS	VARTTI, KELVIN S
09651488	6857049	150	08/30/2000	METHOD FOR MANAGING FLUSHES WITH THE CACHE	VARTTI, KELVIN S.
09650730	6728835	150	08/30/2000	LEAKY CACHE MECHANISM	VARTTI, KELVIN S.
09409756	6374332	150	09/30/1999	CACHE CONTROL SYSTEM FOR PERFORMING MULTIPLE OUTSTANDING OWNERSHIP REQUESTS	VARTTI, KELVIN S.
08579896	5678026	150	12/28/1995	MULTI-PROCESSOR DATA PROCESSING SYSTEM WITH CONTROL FOR GRANTING MULTIPLE STORAGE LOCKS IN PARALLEL AND PARALLEL LOCK PRIORITY AND SECOND LEVEL CACHE PRIORITY QUEUES	VARTTI, KELVIN S.
08180896	5574753	150	01/12/1994	GLITCH FREE CLOCK START/STOP CONTROL CIRCUIT FOR OUTPUTTING A SINGLE CLOCK SIGNAL AND A SINGLE SYNC SIGNAL FROM A PLURALITY OF SYNC SIGNAL INPUTS AND A PLURALITY OF CLOCK SIGNAL INPUTS	VARTTI, KELVIN S.
08163625	5422918	150	12/09/1993	CLOCK PHASE DETECTION SYSTEM FOR DETECTING THE PHASE DIFFERENCE BETWEEN TWO CLOCK PHASES REGARDLESS OF WHICH OF	VARTTI, KELVIN S.

				THE TWO CLOCK PHASES LEADS THE OTHER	
08148246	5381416	150	11/08/1993	DETECTION OF SKEW FAULT IN A MULTIPLE CLOCK SYSTEM	VARTTI, KELVIN S.

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name	First Name	
VARTTI	KELVIN	Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page